

# GeForce6100SM-M2

REV: 1.0A


PCB:15-V09-011010  
BOM:89-206-V09120

MCP61S Real S3  
Components :693PCS  
Add R26.R28.R29.R30  
Del R48

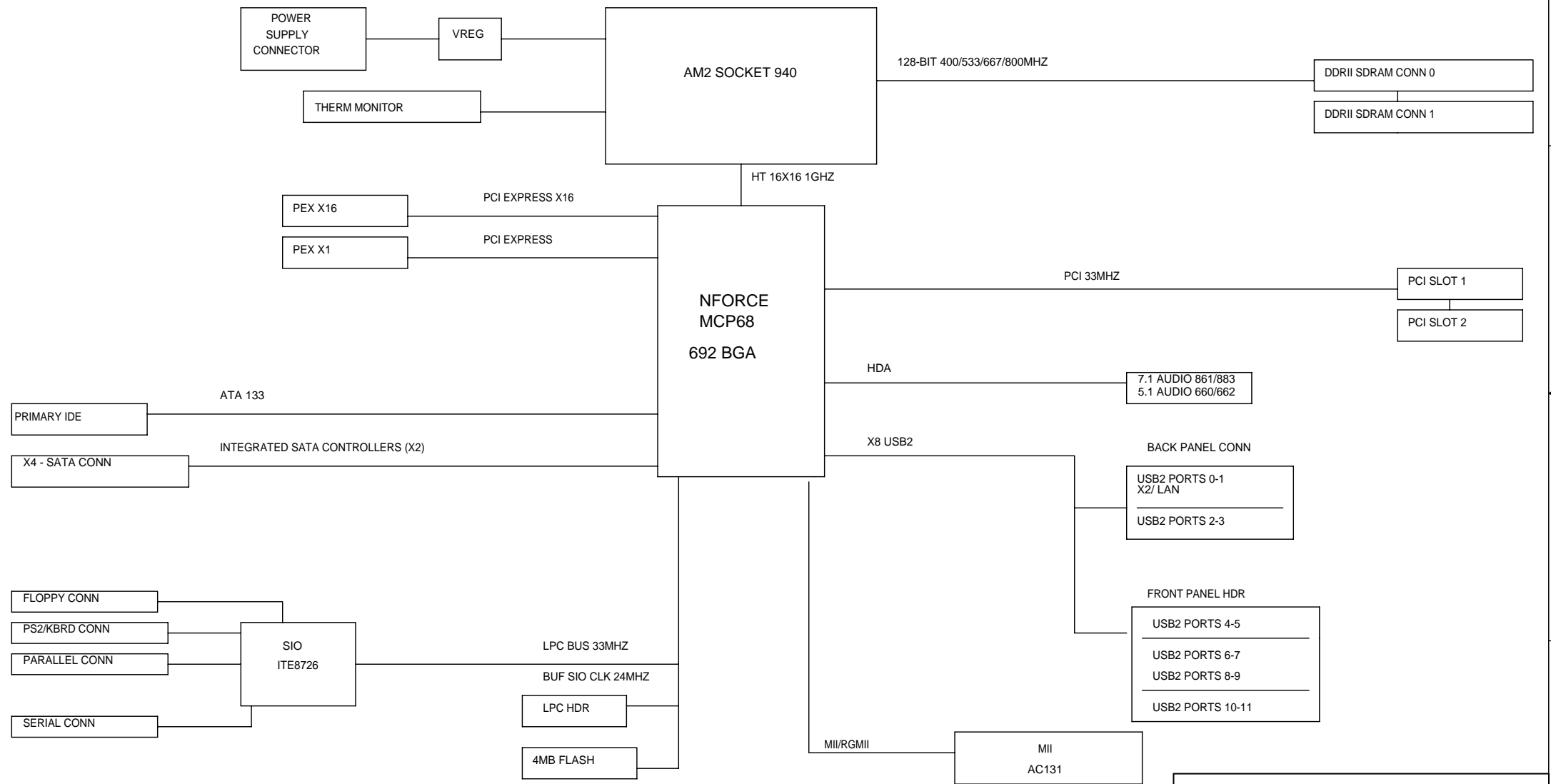
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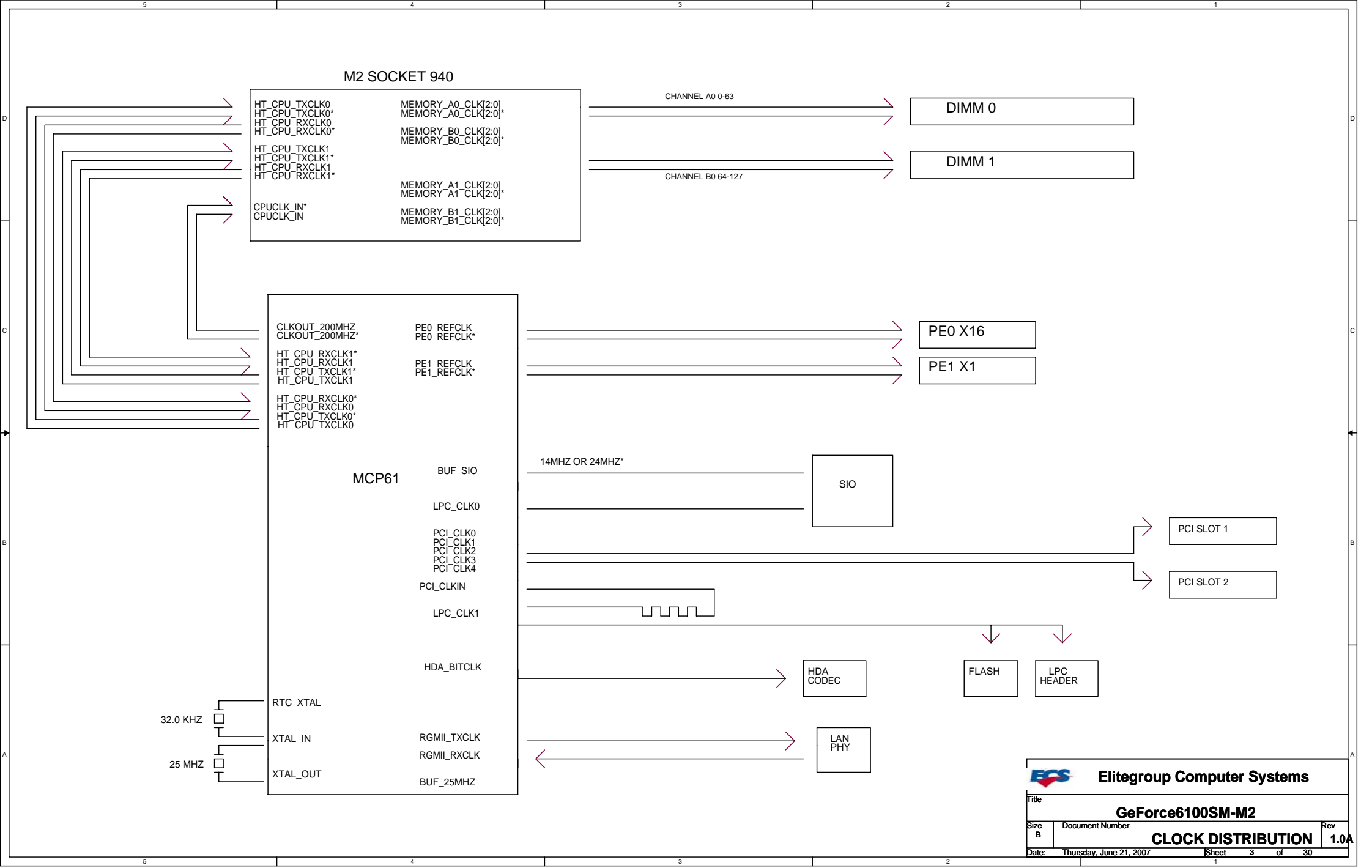
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- 27-PWR CON/FNT PNL
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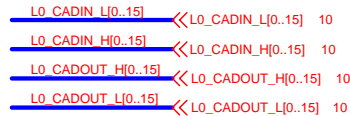
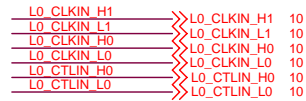
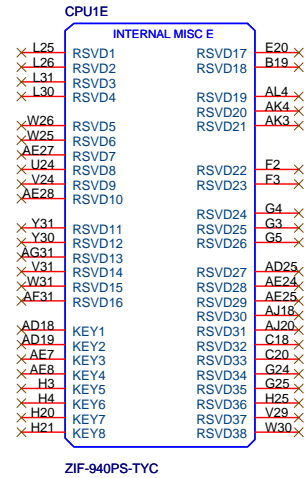
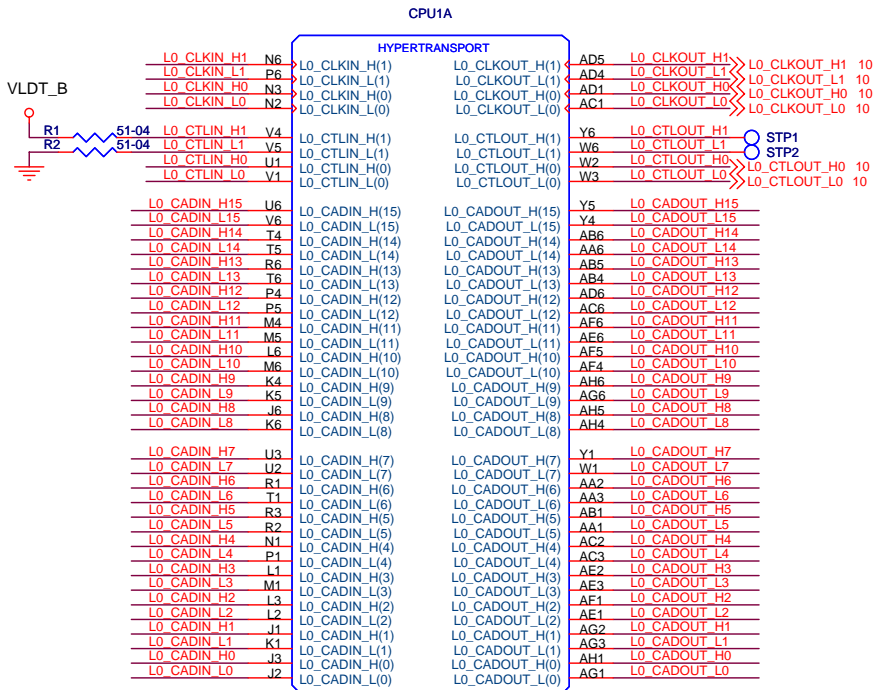
	<i>Signature</i>	<i>Date</i>
<i>Designer</i>	Eli	07/11/2007
<i>Layout</i>	Susan/Angela	05/29/2007
<i>Check</i>		
<i>Approval</i>		

 Elitegroup Computer Systems		
Title GeForce6100SM-M2		
Size B	Document Number COVER PAGE	Rev 1.0A
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# BLOCK DIAGRAM

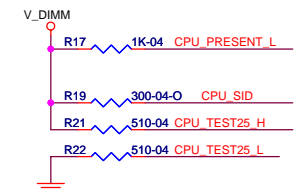
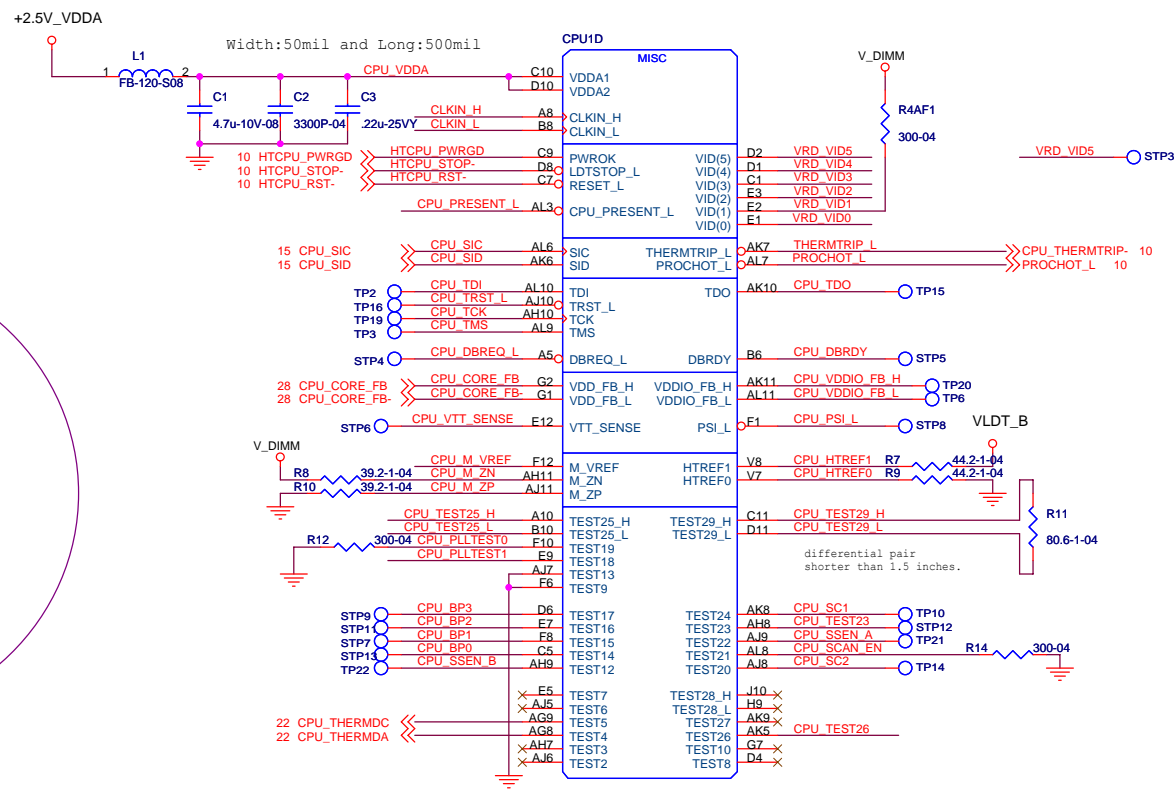
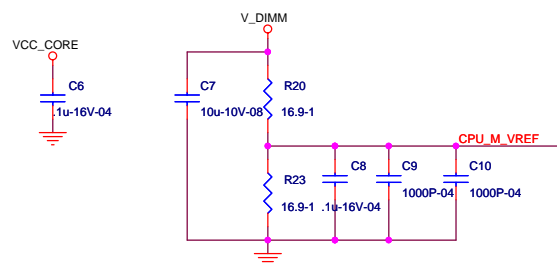
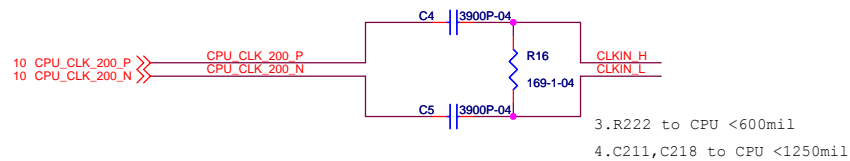
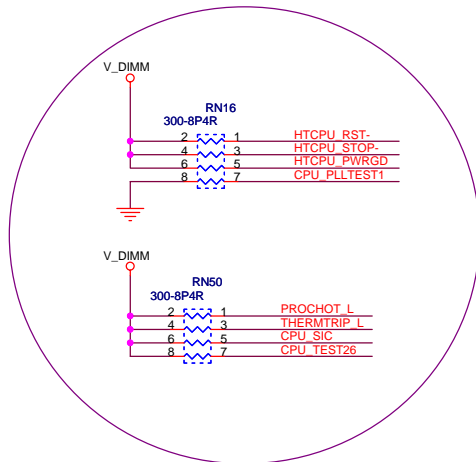


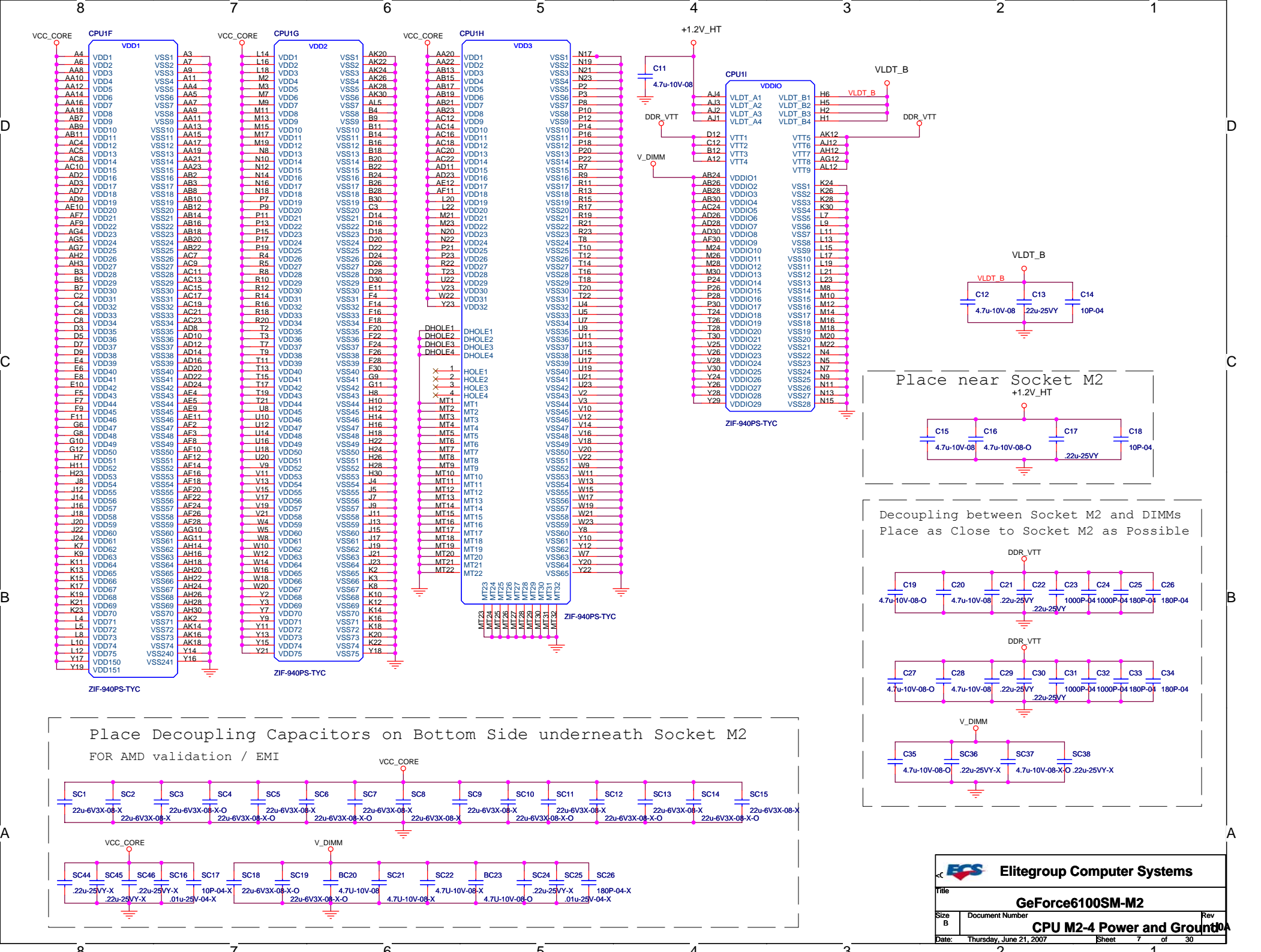




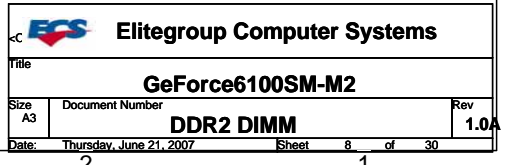


The diagram shows a circuit for generating a 2.5V voltage source. It features an operational amplifier (U2A, GS358SFS) configured as a voltage follower. The non-inverting input (+) is connected to a voltage divider consisting of a 10k resistor (R3) and a 104 resistor, which is connected to a +12V supply. The inverting input (-) is connected to the output of the op-amp. The output of the op-amp (pin 1) is connected to the gate of a MOSFET (Q1, 2N7002-S). The MOSFET's source is connected to ground, and its drain is connected to a +2.5V\_VDDA supply. A 100µF electrolytic capacitor (EC1, 100u-16D6.3H11EG-LU) is connected in parallel with the +2.5V\_VDDA supply to filter the output. The MOSFET is also connected to a +12V supply through a 10k resistor (R3).

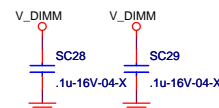
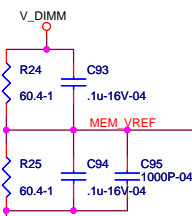
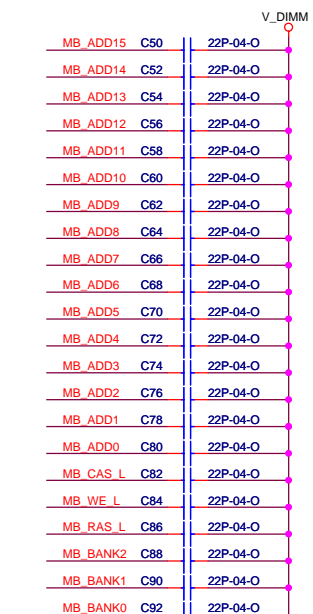
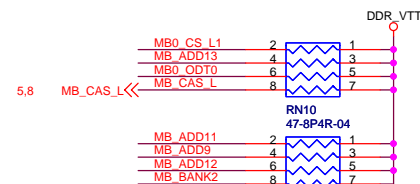
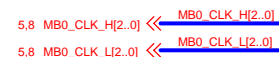
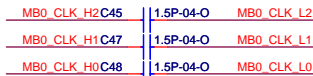
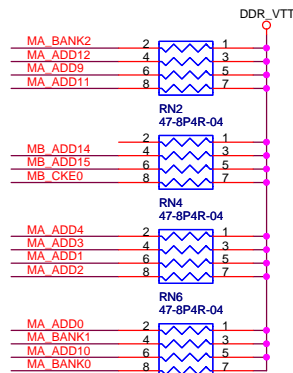
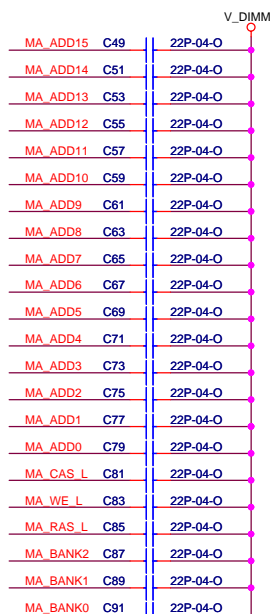
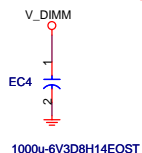
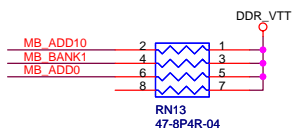
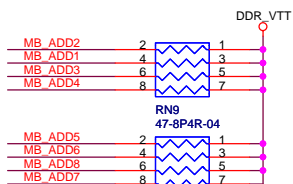
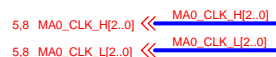
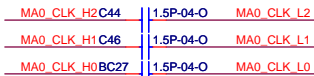
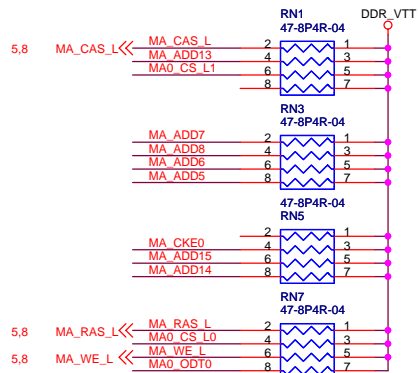






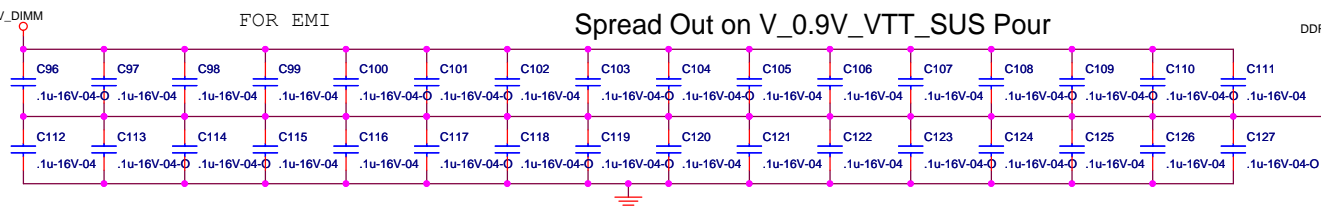






FOR EMI

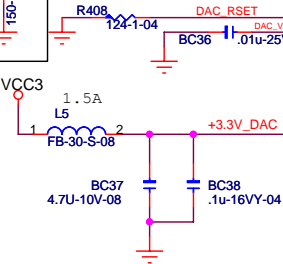
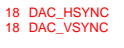
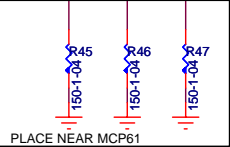
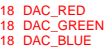
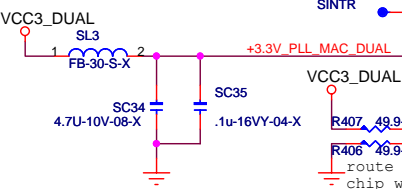
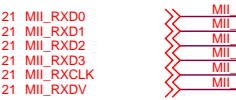
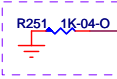
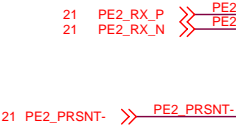
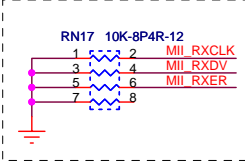
Spread Out on V\_0.9V\_VTT\_SUS Pour





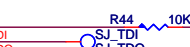
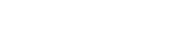
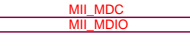
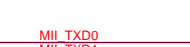
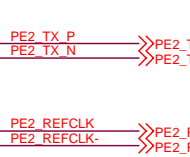
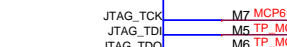
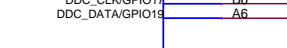
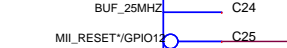
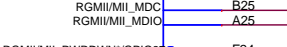
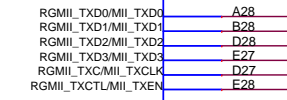
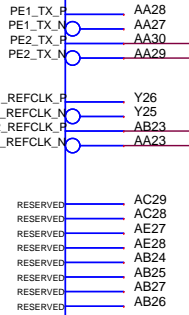
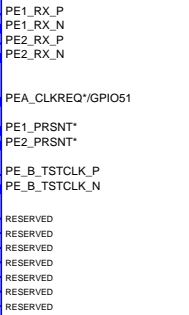


For enhance AC131 Driving



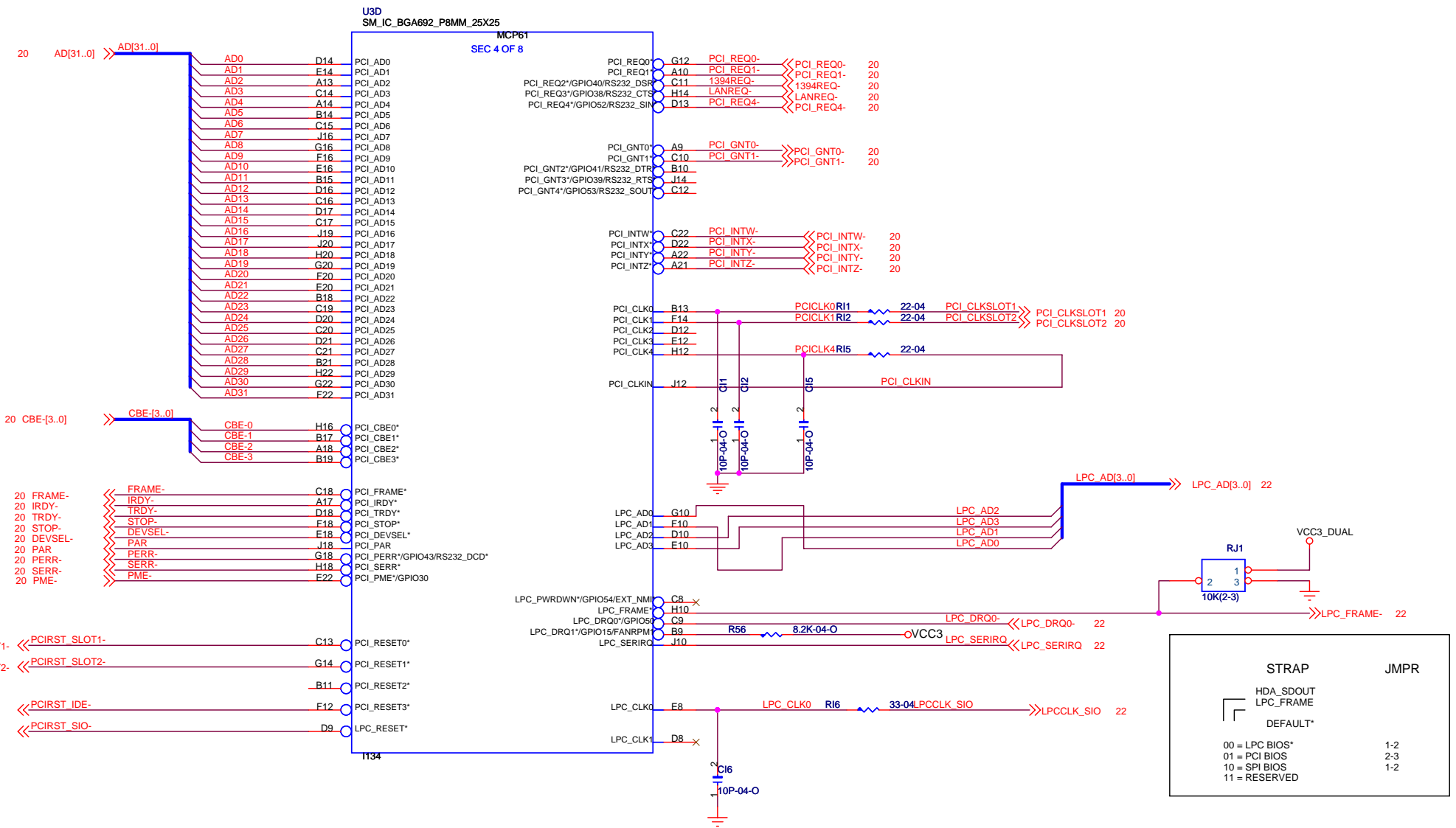
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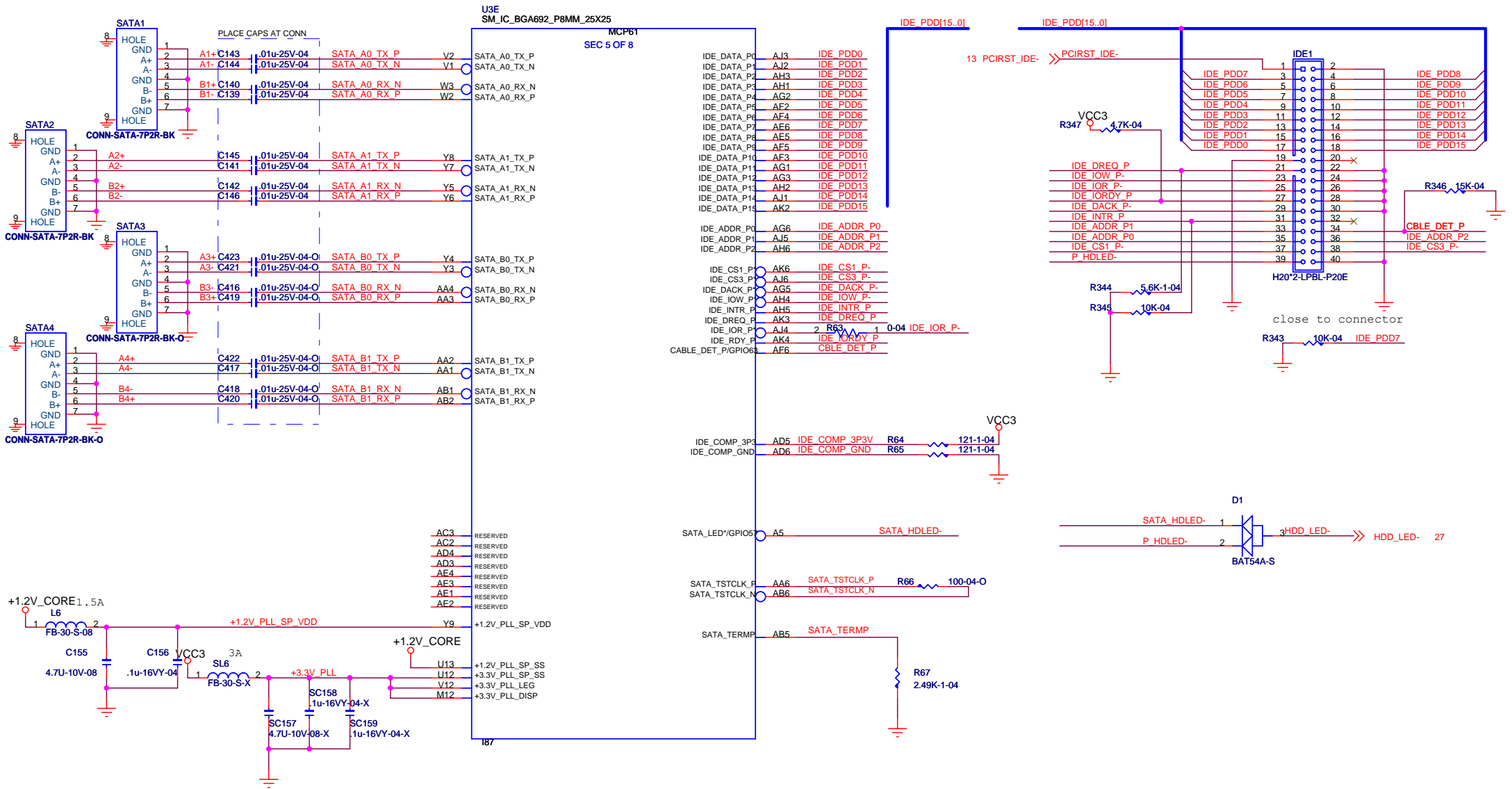
MCP61  
SEC 3 OF 8



Elitegroup Computer Systems

Title			GeForce6100SM-M2		
Size			Document Number		
B			MCP61 PCI-E X1/RGMII/DAC		
Date:			Thursday, June 21, 2007		
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Rev			1.0A		



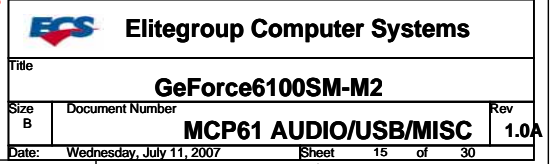


AC\_RST\*  
1 = \*RGMII  
0 = MII

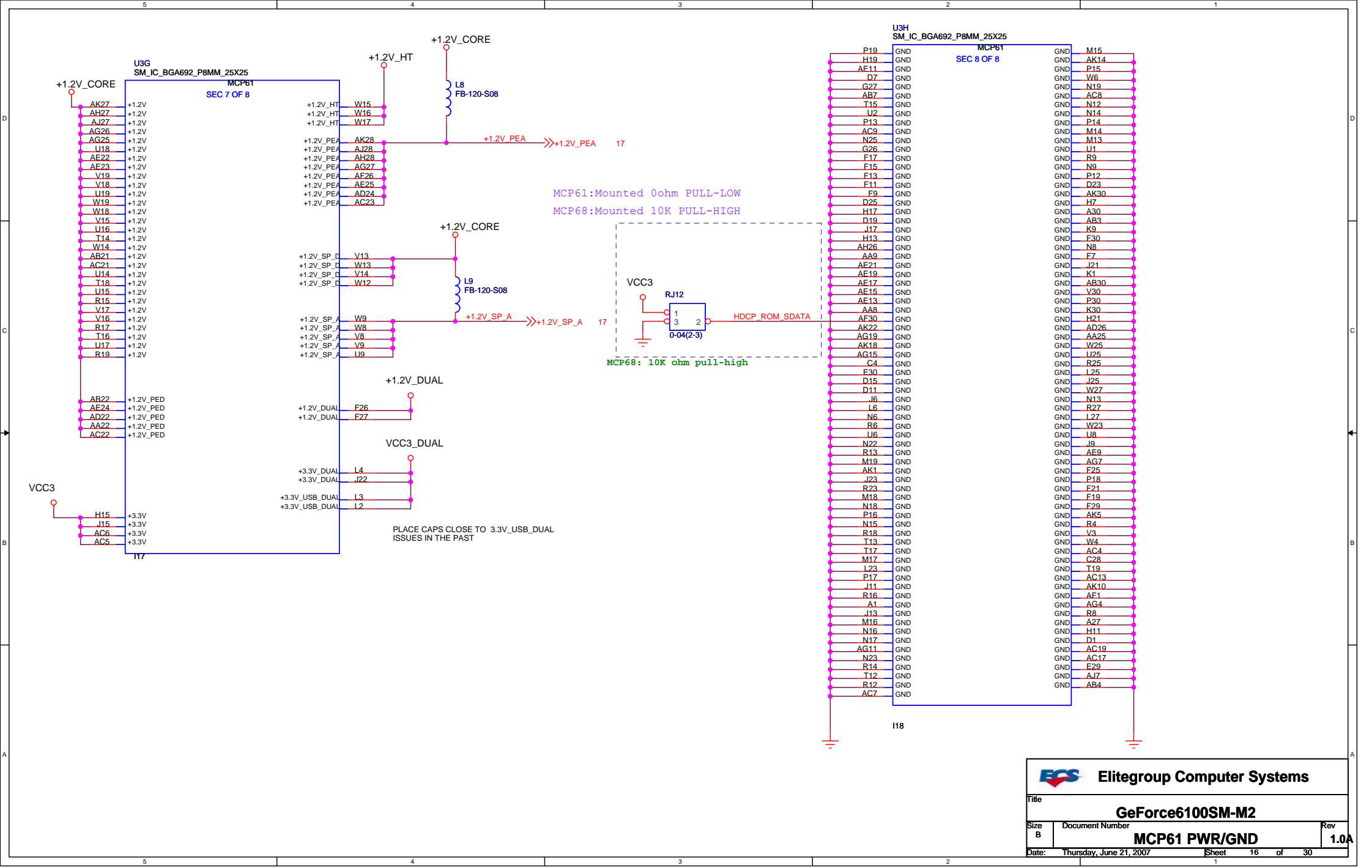
AC\_SYNC  
(SIO CLK)  
1 = \*24MHZ  
0 = 14.318MHZ

\* = DEFAULT

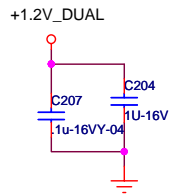
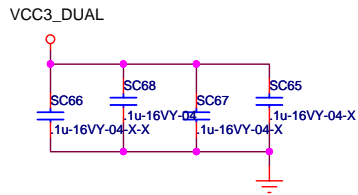
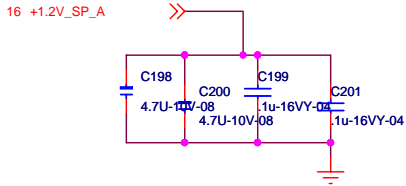
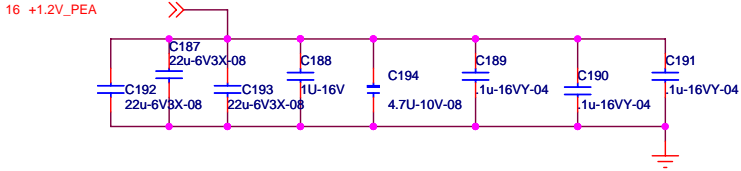
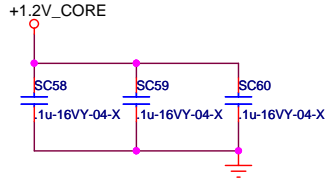
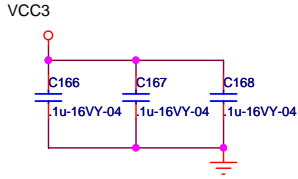
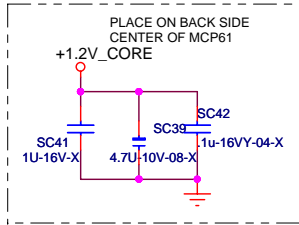
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# MCP61/8 DECOUPLING/EMI



## MCP61 INTERNAL PULL-UP/DWN'S

PE0_PRSENTX16* PE0_PRSENTX8*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_PRSENT* PE2_PRSENT*	10K PU TO 3.3V 10K PU TO 3.3V
PE1_CLKREQ*	10K PU TO 3.3V
PCI_PME*/GPIO_30	8.2K PU TO 3.3V_DUAL
LPC_AD0 LPC_AD1 LPC_AD2 LPC_AD3 LPC_DRQ1/LPC_CS* LPC_DRQ0* LPC_SERIRQ	8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 8.2K PU TO 3.3V 10K PU TO 3.3V
HDA_SDATA_IN1/GPIO_23/MGPIO_0 HDA_SDATA_IN0/GPIO_22	10K PD TO GND 10K PD TO GND
JTAG_TMS JTAG_TRST* JTAG_TDI	10K PU TO 3.3V 10K PD TO GND 10K PU TO 3.3V
A20GATE PE_WAKE* EXT_SMI*/GPIO32 THERM*/GPIO_59 KBRDRSTIN*/GPIO_58 RI*/GPIO_33 SIO_PME*/GPIO_31/MGPIO_2 PWRBTN* RSTBTN*	10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V 10K PU TO 3.3V 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL 10K PU TO 3.3V_DUAL

### MCP61 SPI CLK STRAP

SPI\_DO | SPI\_CLK  
00 = 500KHZ  
01 = 1.8MHZ  
10 = 2.5MHZ  
11 = 25MHZ  
\*DEFAULT

### MCP68 SPI CLK STRAP

SPI\_DO | SPI\_CLK  
00 = 31MHZ  
01 = 42MHZ  
10 = 25MHZ  
11 = 1MHZ  
\*DEFAULT

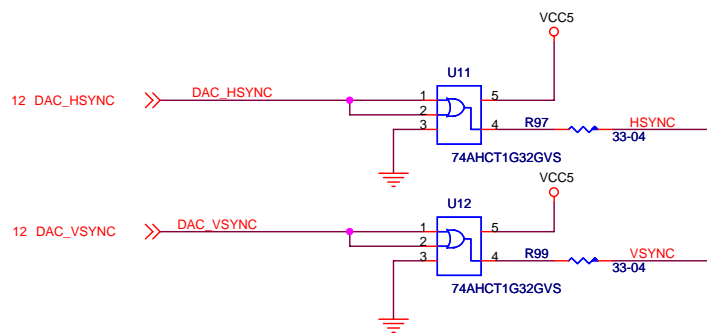
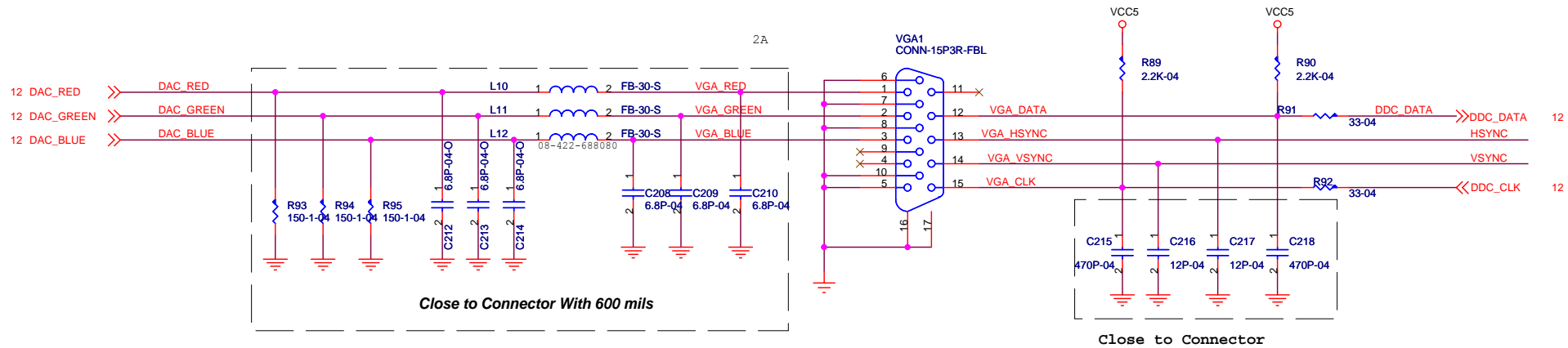
**Elitegroup Computer Systems**

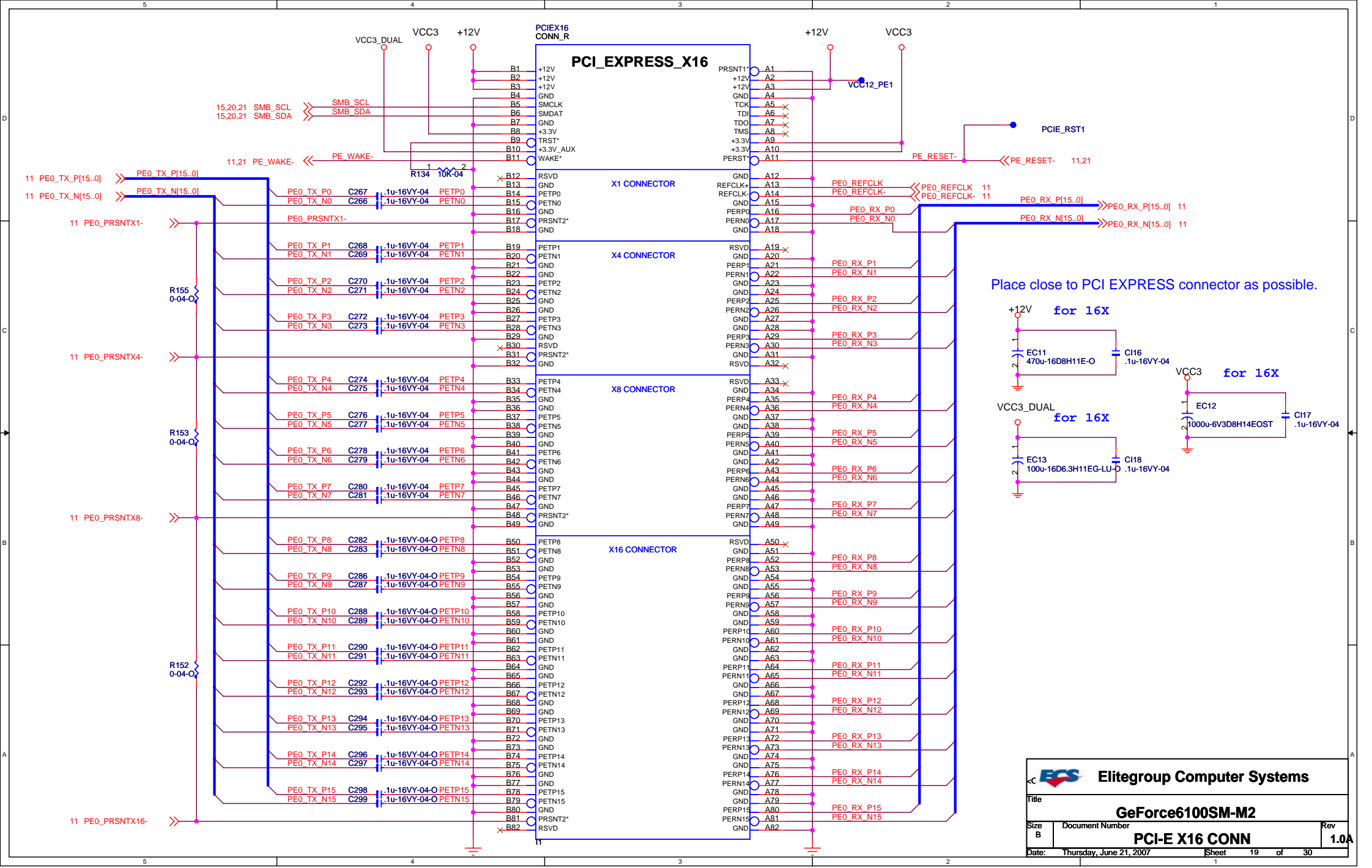
**GeForce6100SM-M2**

**MCP61 SATA / IDE / CONN**

**1.0A**

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 **Sheet** 17 **of** 30







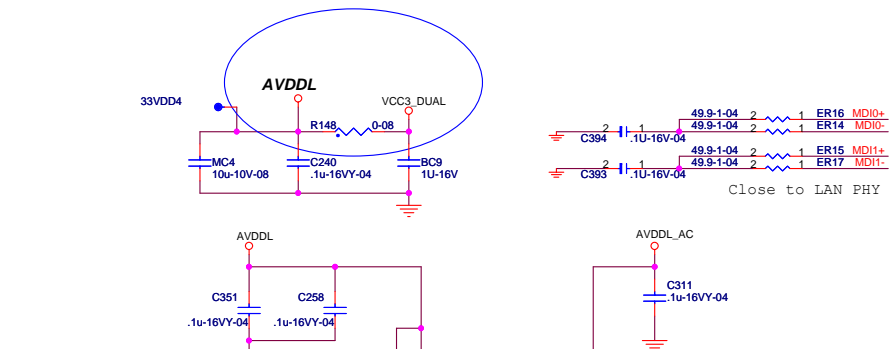
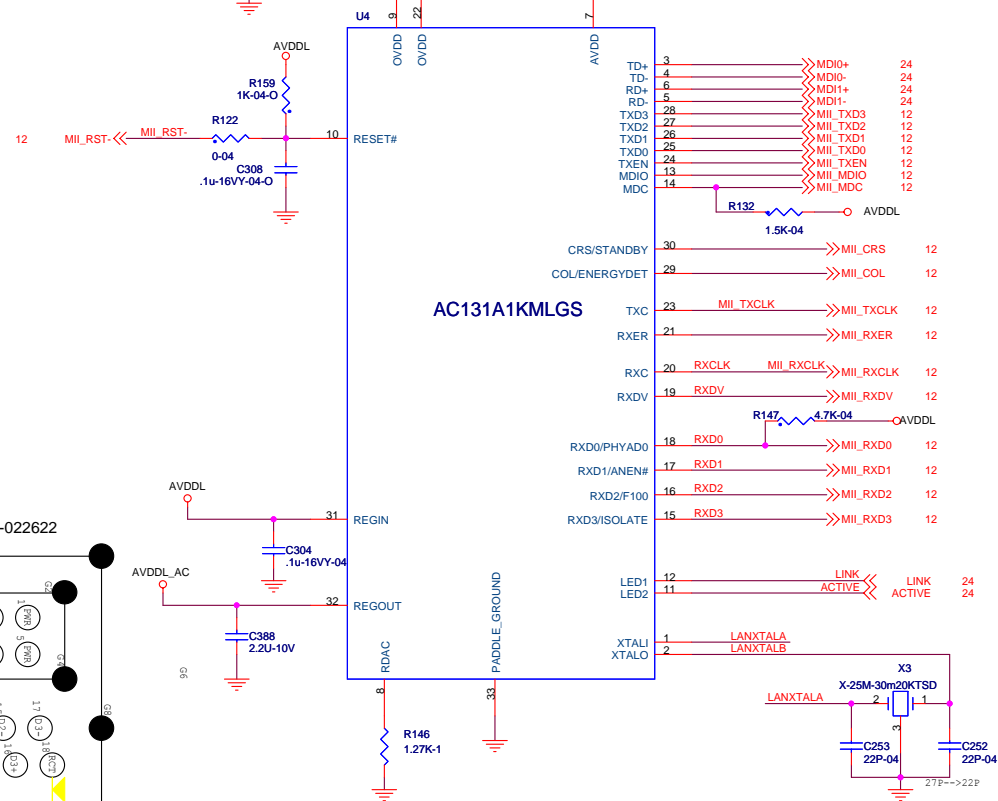
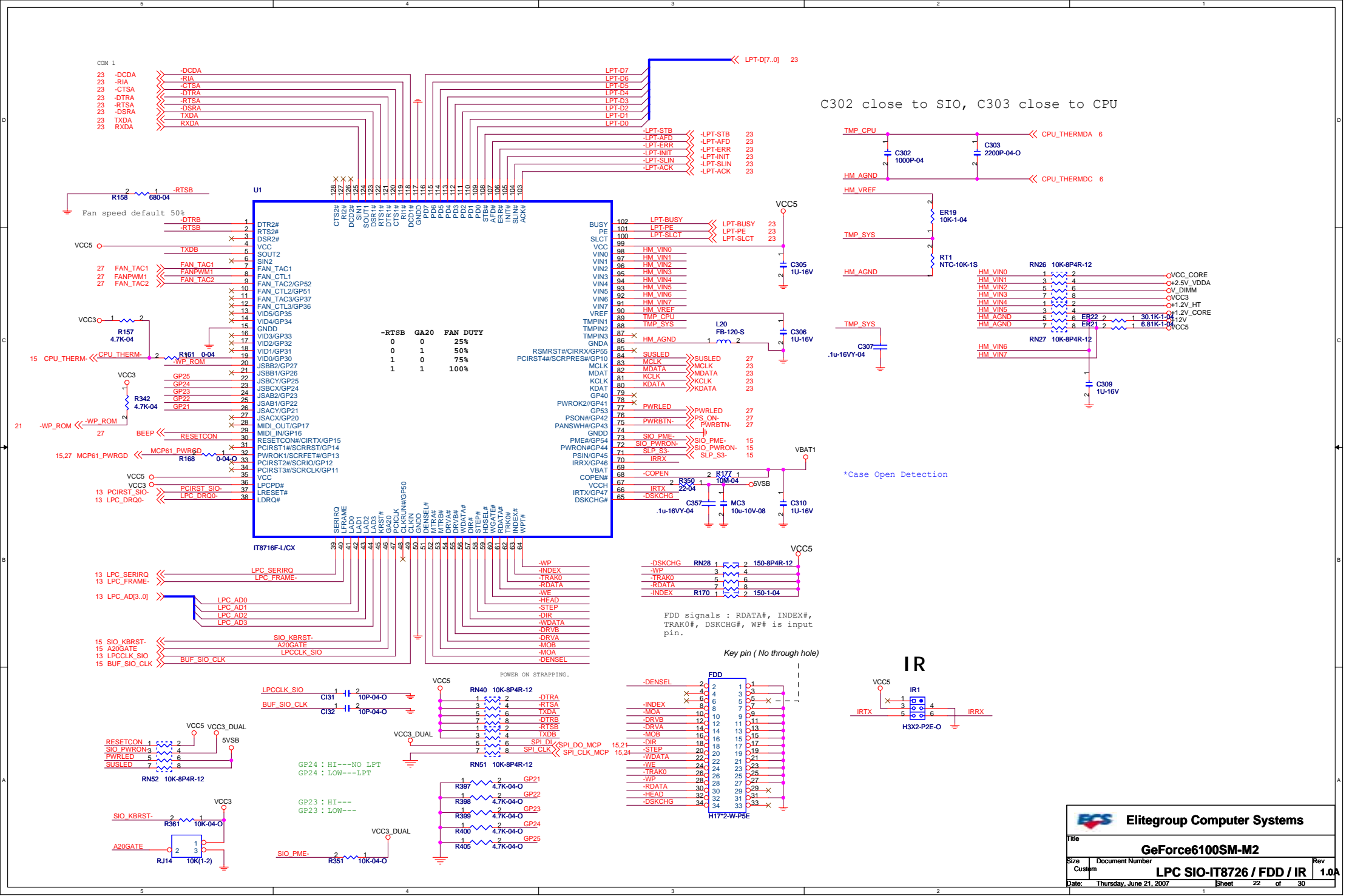
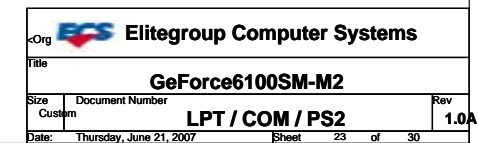
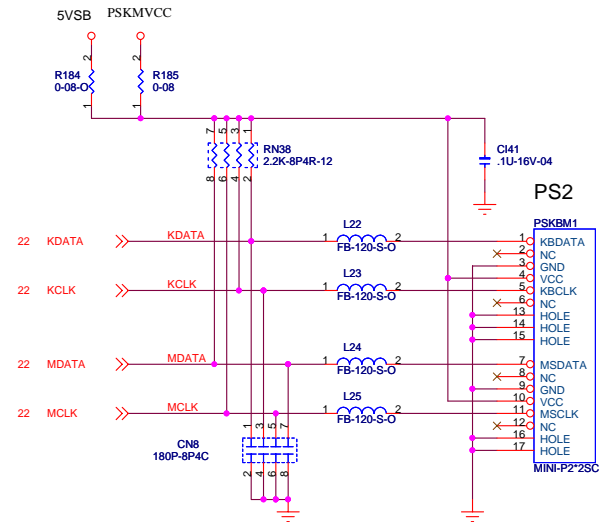
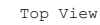
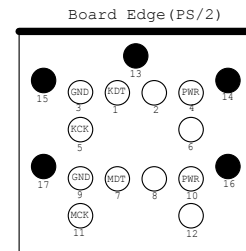


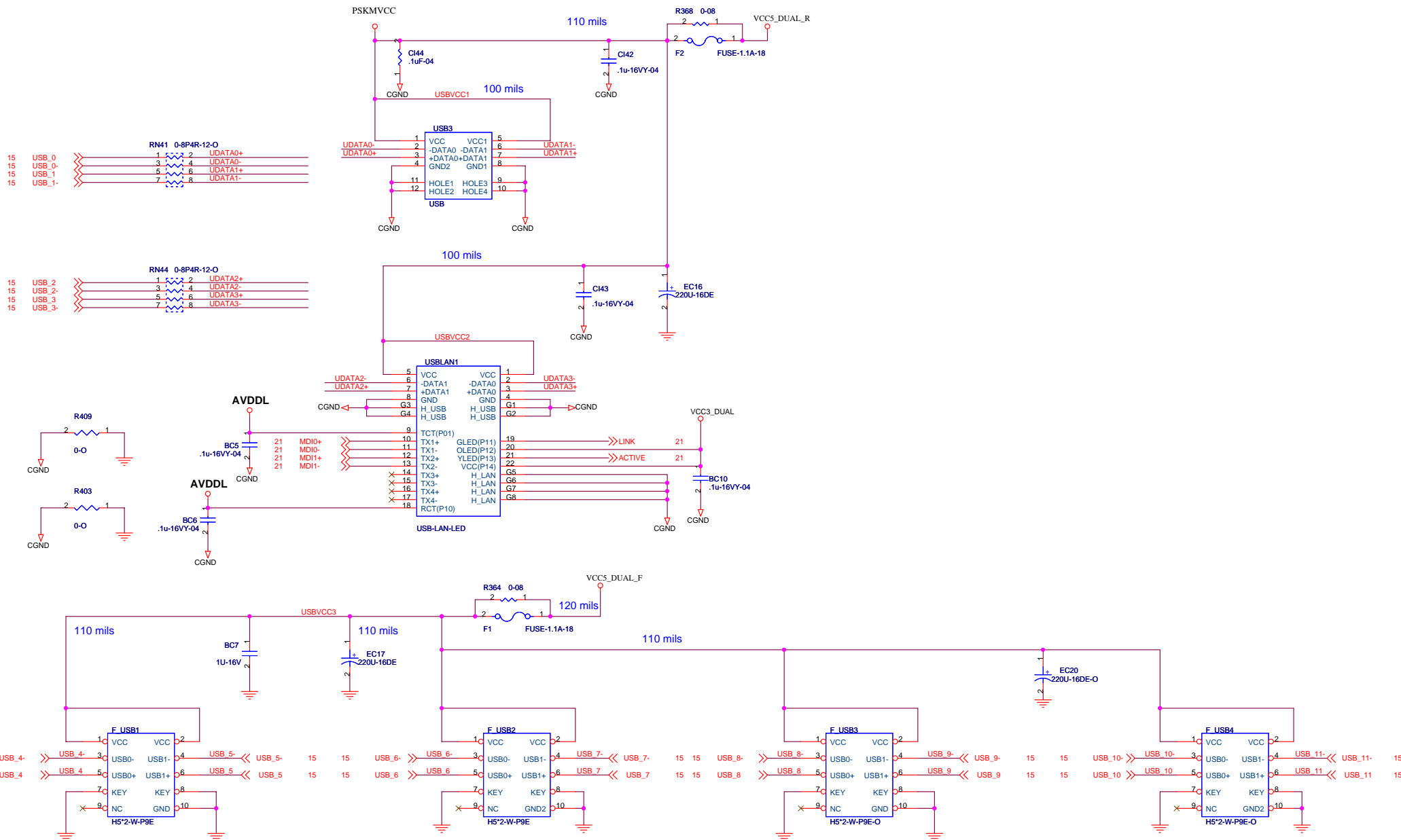
Diagram of a 150 mil package with 16 pins (8 on each side).

[illegible]



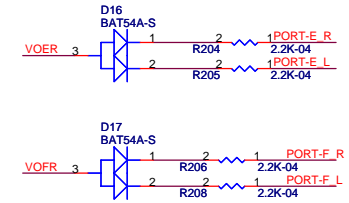
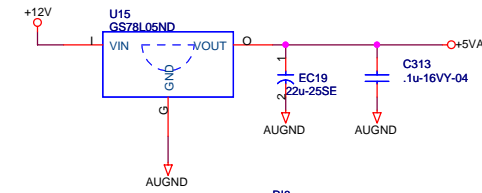






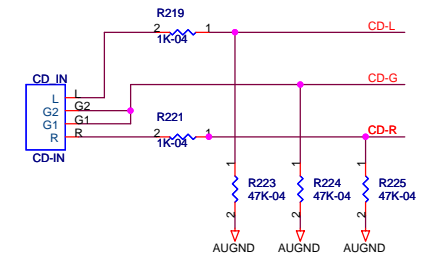
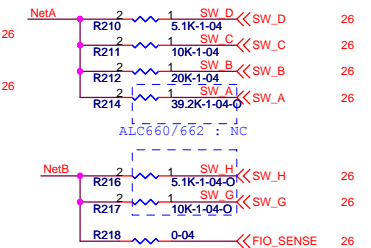
Improve the background noise of MIC boost

### Verfout bias for stereo microphone.

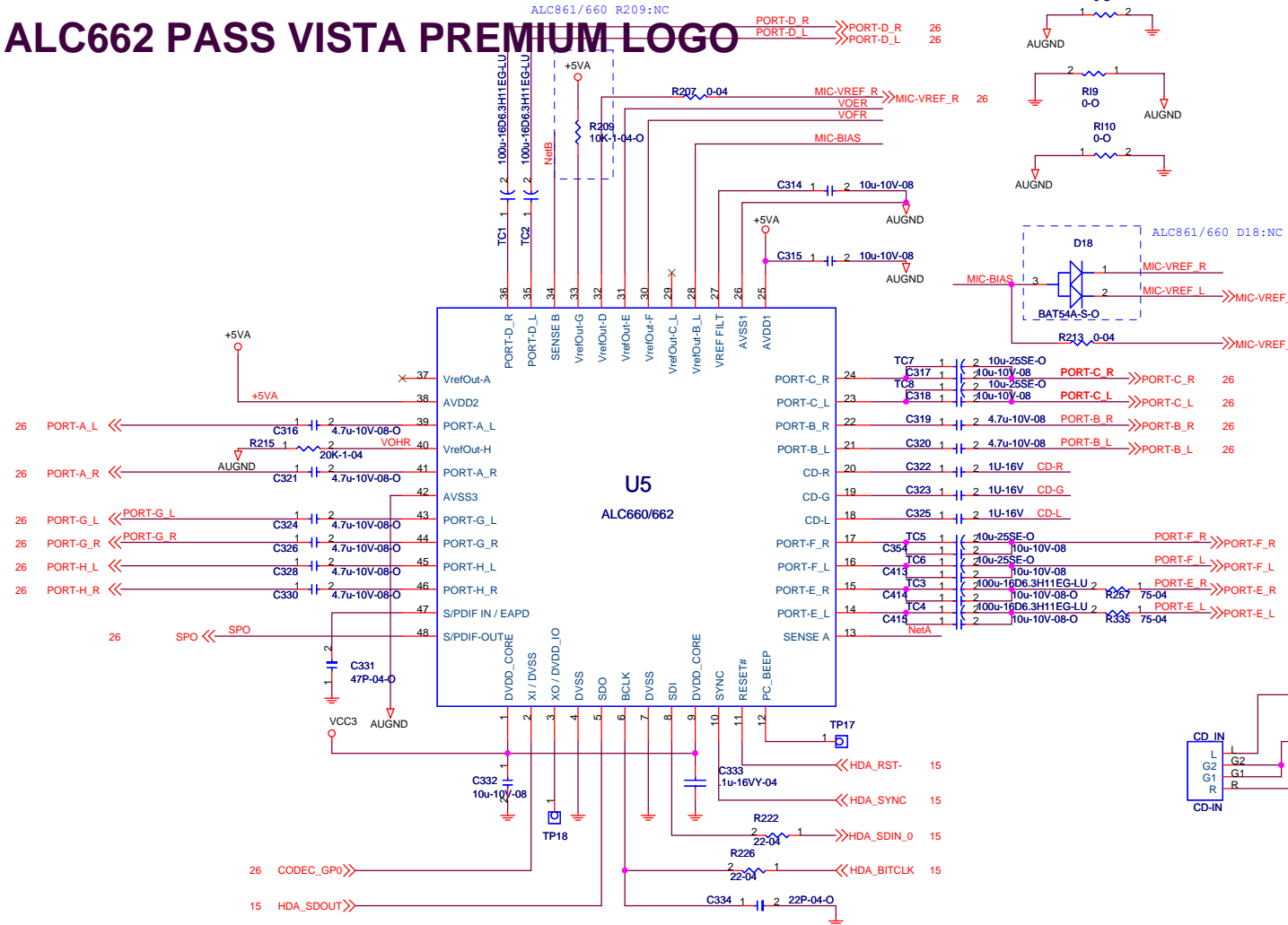


Place near Chip

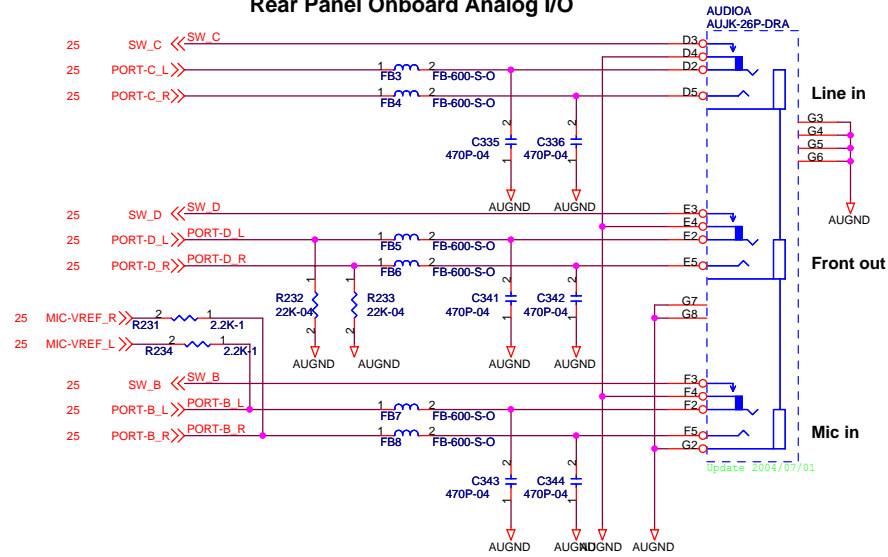
## Resistors Networks



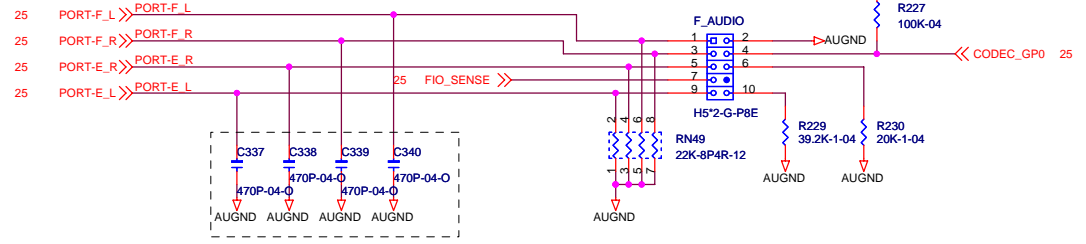
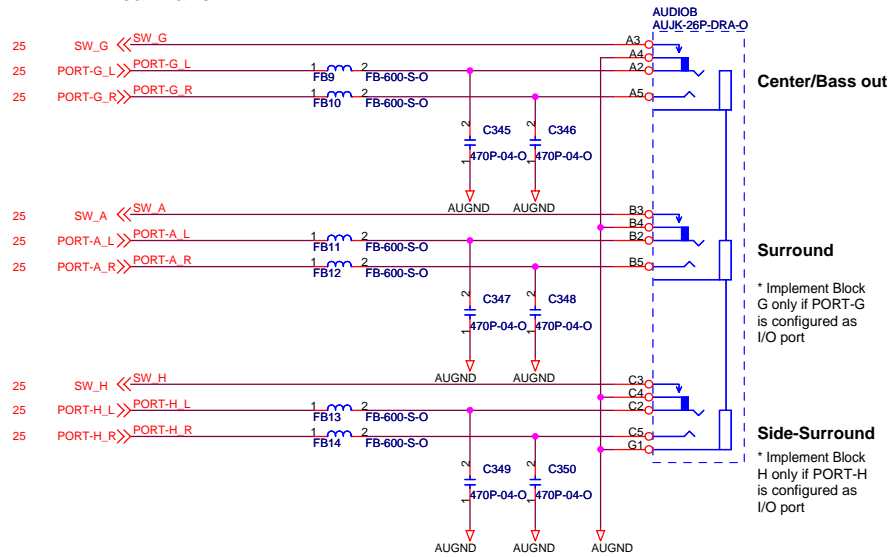
## ALC662 PASS VISTA PREMIUM LOGO



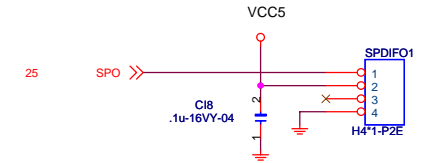
## Rear Panel Onboard Analog I/O



## Rear Panel (Optional Rear Audio Panel)



## SPDIF Out



The schematic should consist with PINs define of I/O connector.

